IN THE CLAIMS:

1. (Previously presented) An error detection system for a clock signal comprising:

a first counter that receives and counts the clock signal,

a phase-locked loop circuit that receives the clock signal and outputs a second clock signal,

a second counter that receives and counts the second clock signal,

a comparator that receives and compares the outputs of the first and the second counters, and

an error output from the comparator that is true when the counts of the first and second counters are unequal.

2. (Previously presented) The error detection system as defined in claim 1 further comprising a second output from the comparator that indicates which counter contains a higher count.

3. (Original) The error detection system as defined in claim 1 further comprising means for resetting the counters synchronized to the successful capture of the clock signal by the PLL.

4. (Previously presented) The error detection system as defined in claim 1 further comprising:

a sender that sends data and the clock signal, the clock signal defined as a forwarding source synchronous clock signal, and

a receiver latch that accepts and latches the data therein with the forwarding clock.

5 (Original) A method for detecting clock signal errors comprising the steps of:

a first counting of the first clock signals,

providing a second clock signal with a frequency that is locked to the average frequency of the first clock signal,

a second counting of the second clock signals,

detecting a difference between the first and the second countings, and

signaling an error therewith.

6. (Original) The method as defined in claim 5 further comprising the step of: signalling which counting is higher.

7 (Previously presented) The method as defined in claim 5 further comprising the step of synchronizing the two countings.

8. (Original) The method as defined in claim 5 further comprising the steps of:

sending data and the clock signal, wherein the clock signal is a forwarding source synchronous clock signal,

receiving the data, and

latching the data with the forwarding clock signal.

9. (Previously presented) A system for detecting errors in a first clock signal, the system comprising:

means for counting the first clock signal,

means, responsive to the first clock signal, for generating a second clock signal,

means for counting the second clock signal,

means for comparing the count of the first clock signal with the count of the second clock signal, and

means for generating an error when the count of the first clock signal differs from the count of the second clock signal.

10. (Previously presented) The system of claim 9 wherein

the first clock signal has an average frequency, and

the second clock signal is locked to the average frequency of the first clock signal.

11. (Previously presented) The system of claim 9 wherein

the first clock signal has a plurality of rising edges and a plurality of falling edges, and

the means for counting the first clock signal counts one of the rising and falling edges.

12. (Previously presented) The system of claim 9 wherein

the first clock signal has a plurality of rising edges and a plurality of falling edges, and

the means for counting the first clock signal counts both the rising and falling edges.

13. (Previously presented) The system of claim 10 wherein the means for generating a second clock signal includes a phase lock loop (PLL) circuit.

14. (Previously presented) The system of claim 9 further comprising means for determining whether the count of the first clock signal is higher or lower than the count of the second clock signal.

15. (New) The system of claim 14 wherein the means for generating a second clock signal includes a phase lock loop (PLL) circuit.

16. (New) The system of claim 14 wherein

the first clock signal has an average frequency, and

the second clock signal is locked to the average frequency of the first clock signal.